MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2015/2016

ECP2046 – COMPUTER ORGANIZATION & ARCHITECTURE

(TE, RE, BE)

10 OCTOBER 2015
9.00 a.m - 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 5 pages including cover page with 5 Questions only.
2. Attempt **ALL FIVE** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.

Question 1

a) State the differences between computer architecture and computer organization. Give 2 examples of architectural attributes and 2 examples of organizational attributes.

[6 marks]

b) The structure of Central Processing Unit (CPU) is formed with 3 interconnected components. Name the 3 major components of CPU. Briefly explain the functions of each components.

[5 marks]

c) What are the functions for each of the following registers?
   i. Program Counter
   ii. Instruction Register
   iii. Address Register
   iv. Data Register
   v. Flag Register

[5 marks]

d) List out 4 techniques that can be used to speed up a processor.

[4 marks]

Question 2

a) Describe the physical characteristics and give an example for each of the following data storage type.
   i. Volatile memory
   ii. Non-volatile memory
   iii. Non-erasable memory

[6 marks]

Continued .....

b) A direct mapped cache consists of 256 lines. In a machine, the cache is used to speed-up main memory access. The main memory consists of 4096 blocks of 64 words each.

i) How is the memory address divided into tag, line, word?

[6 marks]

ii) How will the memory address divided, if a 2-way set associative mapped cache is used instead?

[5 marks]

iii) Name 3 possible replacement algorithms for the set associative mapped cache.

[3 marks]

Question 3

a) Perform the following arithmetic operation using 8-bit two's complement notation.

$$66_{10} - 97_{10}$$

[4 marks]

b) Perform the following arithmetic operation using binary sequential multiplication. Consider the two operands as the unsigned numbers.

$$12_{10} \times 6_{10}$$

[6 marks]

c) Multiply 15.125_{10} with 36.5_{10} using floating point arithmetic. Show how the results would be stored using IEEE 32-bit floating-point format.

[10 marks]

Continued .....

Question 4

a) Given the following assembly program

```
MOV  R0, 5H
MUL  R0, [10H]
ADD  A, R0
MOV  R1, A
```

i) Name the addressing mode for each of the instruction, by considering only the right-most operand.

[4 marks]

ii) Provided the initial values for the following registers and memory location,

Register	Value
A	40H
R0	00H
R1	00H

Memory Address	Value
5H	21H
10H	12H

what are the values in the registers and memory location after the execution of the 4 instructions?

[5 marks]

iii) By labeling [10H] as X, write out the mathematical expression representing the program.

[2 marks]

Continued .....

b) Given the following operations can be performed by ALU,

- add 2 input registers
- complement the bits of any register
- increment any register
- decrement any register

list in order the micro-operations the control unit must perform the following instruction:

SUB R0, R1

[5 marks]

c) Give the 3 advantages and 1 disadvantage of micro-programmed control unit over hardwired control unit.

[4 marks]

Question 5

a) With the aid of diagrams, explains how superpipeline and superscalar can be used to enhance the performance of a 4-stage pipeline. The following lists the 4 stages of the pipeline.

- Instruction Fetch (IF)
- Instruction Decode (ID)
- Instruction Execution (IE)
- Write Operation (WO)

If 6 instructions are to be executed, how many clock cycles are needed for pipeline, superpipeline and superscalar? Assume no instruction branching occurs.

[4 + 3 + 3 marks]

b) Name 5 fundamental limitations of superscalar, and briefly explain them.

[10 marks]

End of Page